Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. An operation method of a phase lock loop circuit, comprising:
obtaining a first value and a second value by respectively counting an input signal with a first frequency received by the phase lock loop circuit within one cycle period and counting an output signal with a second frequency from a voltage control oscillator within the same cycle period;
obtaining a third value by comparing the difference of the first value and the second value and forwarding to the voltage control oscillator; and
modifying the second frequency of the output signal in response to the third value for the phase lock loop circuit and forwarding to a counter until the difference of the first value and the second value is substantial zero.

[c2] 2. The operation method of a phase lock loop circuit as claimed in claim 1, wherein the speed of modifying the second frequency of the output signal of the voltage control oscillator varies with the third value, wherein when the third value becomes larger, the speed of modifying the second frequency of the output signal becomes

faster, when the third value becomes smaller, the speed of modifying the second frequency of the output signal becomes slower.

[c3] 3. The operation method of a phase lock loop circuit as claimed in claim 1, wherein before obtaining the first value, the first frequency of the input signal received by the phase lock loop circuit is further divided by a first frequency divider with a first number and the first value is obtained in response to the divided first frequency of the input signal.

[c4] 4. The operation method of a phase lock loop circuit as claimed in claim 3, wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is further divided by a second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.

[c5] 5. The operation method of a phase lock loop circuit as claimed in claim 1, wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is further divided by a second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.

[c6] 6. The operation method of a phase lock loop circuit as claimed in claim 1, wherein before modifying the second frequency of the output signal in response to the third value, the third value is further filtered by a loop filter to filter out a high frequency noise existed in the phase lock loop circuit.

[c7] 7. The operation method of a phase lock loop circuit as claimed in claim 1, wherein the input signal with the first frequency is generated by a crystal oscillator.

[c8] 8. The operation method of a phase lock loop circuit as claimed in claim 1, wherein combination of the step of calculating the first frequency of the input signal received by the phase lock loop circuit and the step of dividing the first frequency of the input signal are performed by a programmable counter.

[c9] 9. A phase lock loop circuit, comprising:
a counter, for obtaining a first value and a second value by respectively counting an input signal with a first frequency received by the phase lock loop circuit within one cycle period and counting an output signal with a second frequency within the same cycle period, wherein a third value is obtained by comparing the difference of the first value and the second value; and

a voltage control oscillator for generating the output signal, wherein when the voltage control oscillator obtains the third value from the counter, modifying the frequency of the output signal in response to the third value for the phase lock loop circuit.

[c10] 10. The phase lock loop circuit as claimed in claim 9, wherein the speed of modifying the second frequency of the output signal of the voltage control oscillator varies with the third value, wherein when the third value becomes larger, the speed of modifying the second frequency of the output signal becomes faster, when the third value becomes smaller, the speed of modifying the second frequency of the output signal becomes slower.

[c11] 11. The phase lock loop circuit as claimed in claim 9, further comprising a first frequency divider, wherein before obtaining the first value, the first frequency of the input signal received by the phase lock loop circuit is further divided by the first frequency divider with a first number and the first value is obtained in response to the divided first frequency of the input signal.

[c12] 12. The phase lock loop circuit as claimed in claim 11, further comprising a second frequency divider, wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is

further divided by the second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.

[c13] 13. The phase lock loop circuit as claimed in claim 9, further comprising a second frequency divider, wherein before obtaining the second value, the second frequency of the output signal from the voltage control oscillator is further divided by a second frequency divider with a second number and the second value is obtained in response to the divided second frequency of the output signal.

[c14] 14. The phase lock loop circuit as claimed in claim 9, further comprising a loop filter, located between the counter and the voltage control oscillator, wherein before modifying the second frequency of the output signal in response to the third value, the third value is further filtered by the loop filter to filter out a high frequency noise existed in the phase lock loop circuit.

[c15] 15. The phase lock loop circuit as claimed in claim 9, wherein the input signal with the first frequency is generated by a crystal oscillator.

[c16] 16. The phase lock loop circuit as claimed in claim 9,

wherein the counter and a first frequency divider are combined together to form a programmable counter for generating various frequencies.